

"Implementation of Adaptive Digital Controllers on Programmable Logic Devices"

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Much has been made of the capabilities of FPGA's in the hardware implementation of fast digital signal processing functions. Such capability also makes an FPGA a suitable platform for the digital implementation of closed loop controllers. Other researchers have implemented a variety of closed-loop digital controllers on FPGA's. Some of these controllers include the widely used proportional-integral-derivative (PID) controller, state space controllers, neural network and fuzzy logic based controllers. There are myriad advantages to utilizing an FPGA for discrete-time control functions which include the capability for reconfiguration when SRAM-based FPGA's are employed, fast parallel implementation of multiple control loops and implementations that can meet space level radiation tolerance requirements in a compact form-factor. Generally, a software implementation on a DSP device or microcontroller is used to implement digital controllers. At Marshall Space Flight Center, the Control Electronics Group has been studying adaptive discrete-time control of motor driven actuator systems using digital signal processor (DSP) devices. While small form factor, commercial DSP devices are now available with event capture, data conversion, pulse width modulated (PWM) outputs and communication peripherals, these devices are not currently available in designs and packages which meet space level radiation requirements. In general, very few DSP devices are produced that are designed to meet any level of radiation tolerance or hardness. The goal of this effort is to create a fully digital, flight ready controller design that utilizes an FPGA for implementation of signal conditioning for control feedback signals, generation of commands to the controlled system, and hardware insertion of adaptive control algorithm approaches. An alternative is required for compact implementation of such functionality to withstand the harsh environment encountered on spacecraft. Radiation tolerant FPGA's are a feasible option for reaching this goal.



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Adaptive Control



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- Adaptive control is used for the control of systems having dynamics which vary over time or with operating conditions
- In the types of controllers considered to be adaptive, Astrom and Wittenmark include Gain Scheduling, Model Reference Adaptive Control and Self-Tuning Regulators[1]
- This work is primarily concerned with the Self-Tuning Regulator developed by Astrom and Wittenmark



Adaptive Control



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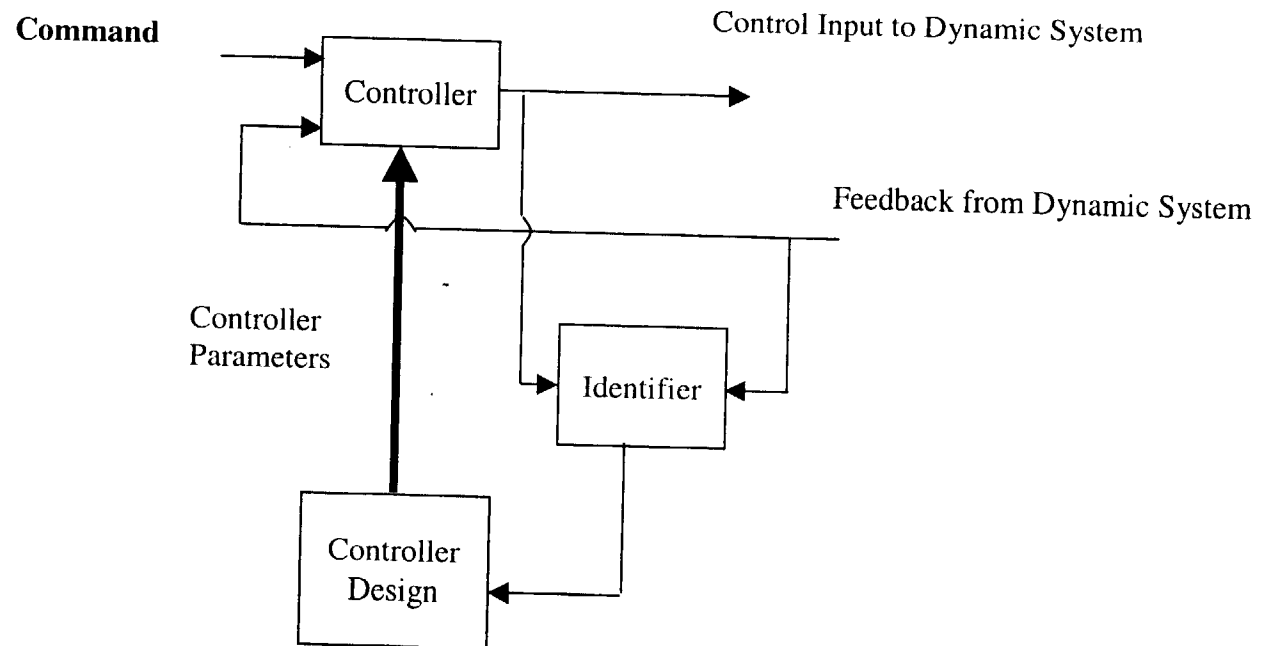


Diagram of a Self-tuning Regulator



Adaptive Control



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- Self-tuning regulators combine a linear controller with a parameter identification approach to provide a structure in which the gains of the controller are calculated on-line.
- Applications of interest are electromechanical actuators (EMA's) currently in use on spacecraft, and those proposed for a power-by-wire system. For example;
 - » Aero Control Surface Positioning
 - » Thrust Vector Control
 - » Valve Positioning
 - » Motor-driven Pumps
 - » Translation systems for space-borne experiments



Adaptive Control



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- Why use adaptive control for actuators?
 - » Open literature and current observation indicate the vast majority of EMA controllers employ a linear control approach with fixed gains[2,3,4,5,6]
 - Tuning may not be optimal due to uncertainty in system parameters, i.e. inertia, damping or load torque.
 - Cannot accommodate changes in actuator dynamics due to wear and tear and operation at loads outside the expected range
 - » On-line adaptive control addresses these shortcomings and increases the “intelligence” of a closed loop control system.
 - Improved control system performance in the face of unanticipated changes in actuator/mechanical system dynamics
 - Self-tuning of actuator control loops
 - System parameter identification can be used in a fault-detection and isolation scheme



Implementation of Adaptive Control



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- Actuator or subsystem-level digital controllers are frequently implemented using digital signal processors (DSP's)
 - » DSP's are designed to perform repetitive, math intensive operations, (i.e. FIR or IIR filters, FFT)
 - » Manufacturers such as Texas Instruments, Analog Devices and Motorola are producing mixed-signal DSP devices that include peripherals for analog-to-digital conversion, event-capture, quadrature signal decoding, PWM outputs and serial communications
 - » Adaptive control can easily be implemented in software on DSPs, or on other microprocessors with suitable execution speed.
 - » This has been done in a laboratory environment at MSFC[7]



FPGA Implementation of Controllers



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- Many examples of digital controller implementation on an FPGA exist. Some of these are;
 - » PID Controller for wheel speed control as part of a digital controller for a wheelchair [8]
 - » Implementation of controllers for robotic applications[9]
 - » Direct torque control of an induction motor[10]
 - » Neural Network implementation for control of an induction motor[11]
 - » Implementation of a Kalman Filter and Linear Quadratic Gaussian controller applied to control of an inverted pendulum[12],[13]
 - » Fuzzy logic controller for a variable speed generator[14]



FPGA Implementation of Controllers



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- In the referenced papers, the FPGA approach for implementation of digital controllers is selected because;
 - » SRAM Based FPGA's provide reconfigurable hardware designs
 - » FPGA's can process information faster than a general purpose DSP
 - » Controller architecture can be optimized for space or speed
 - » Bit widths for data registers can be selected based on application needs
 - » Implementation in VHDL or Verilog allows the targeting of a variety of commercially available FPGA's
- Implementation of digital controllers in FPGA's for space applications is attractive because
 - » FPGA's are available in radiation tolerant packages, whereas availability of radiation tolerant DSP devices is extremely limited
 - » Complex, digital control operations and controller interface peripherals can both be contained in a compact form factor
 - » Multiple digital control loops in one FPGA can replace analog control loops implemented in many space consuming and power hungry radiation tolerant analog IC's

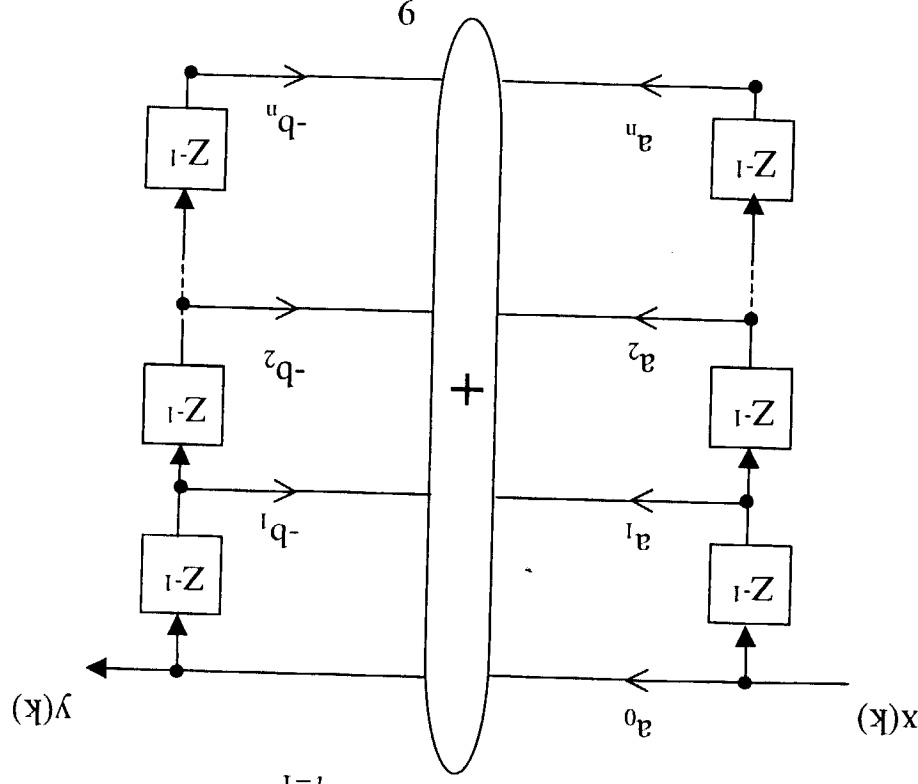


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Digital Controllers

➤ Digital controllers can be implemented as digital filters in the following form[15], where k is the current sample in time, for a given sample period T ;

$$y(k) = \sum_{i=0}^n a_i x(k-i) - \sum_{i=1}^n b_i y(k-i)$$



Z^{-1} Blocks are
Delays of
one sample
period

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Digital Controllers



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- With $n = 2$, a second order filter is obtained which can be used to implement second order controllers or cascaded to create higher order controllers[15].

In the sampled time domain,

$$y(k) = a_0x(k) + a_1x(k-1) + a_2x(k-2) - b_1y(k-1) - b_2y(k-2)$$

The z-transformed transfer function is ,

$$D(z) = \frac{Y(z)}{X(z)} = \frac{a_0 + a_1z^{-1} + a_2z^{-2}}{1 + b_1z^{-1} + b_2z^{-2}}$$



Digital Controllers



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- The well known PID Controller can be implemented using a second order digital filter[15].

In continuous time the PID Controller is represented by

$$u(t) = K_p e(t) + \frac{1}{(K_I)} \int e(t) dt + K_D \frac{de(t)}{dt}$$

For implementation in a discrete time system, with sampling time T, the PID controller is,

$$u(k) = K_p e(k) + \frac{T}{K_I} S(k) + K_D \frac{e(k) - e(k-1)}{T}$$

$$S(k) = S(k-1) + \frac{T}{2} [e(k) + e(k-1)]$$

The z-transform of this function is

$$D(z) = K_p + \frac{K_I T}{2} \left(\frac{z+1}{z-1} \right) + \frac{K_D}{T} \left(\frac{z-1}{z} \right)$$



Digital Controllers



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- With some manipulation, the z-transform of the PID controller can be represented as a second order transfer function[15]

$$D(z) = \frac{(K_P + K_I T / 2 + K_D / T) + (-K_P + K_I T / 2 - 2K_D / T)z^{-1} + K_D / T z^{-2}}{1 - z^{-1}}$$

$$D(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}}$$

$$a_0 = K_P + \frac{K_I T}{2} + \frac{K_D}{T}$$

$$b_1 = -1$$

$$a_1 = -K_P + \frac{K_I T}{2} - \frac{2K_D}{T}$$

$$b_2 = 0$$

$$a_2 = \frac{K_D}{T}$$



Self-Tuning Controller



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- For this work, the Self-Tuning Regulator, due to Astrom and Wittenmark [1], will be referred to as a Self-Tuning Controller;
 - » “Regulation” implies the rejection of disturbances to maintain a controlled process at a constant setpoint, while “control” implies the broader action of following a desired trajectory and rejecting disturbances
 - » This controller makes use of a general linear controller, shown as a z-transform below, where u_c is the desired trajectory, y is the controlled process output and u is the control input to the process.
 - » The coefficients of R , T and S calculated using pole placement design to produce the desired closed-loop response

$$R(z)U(z) = T(z)U_c(z) - S(z)Y(z)$$



Self-Tuning Controller



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When the process output is sampled with period T , it can be represented as

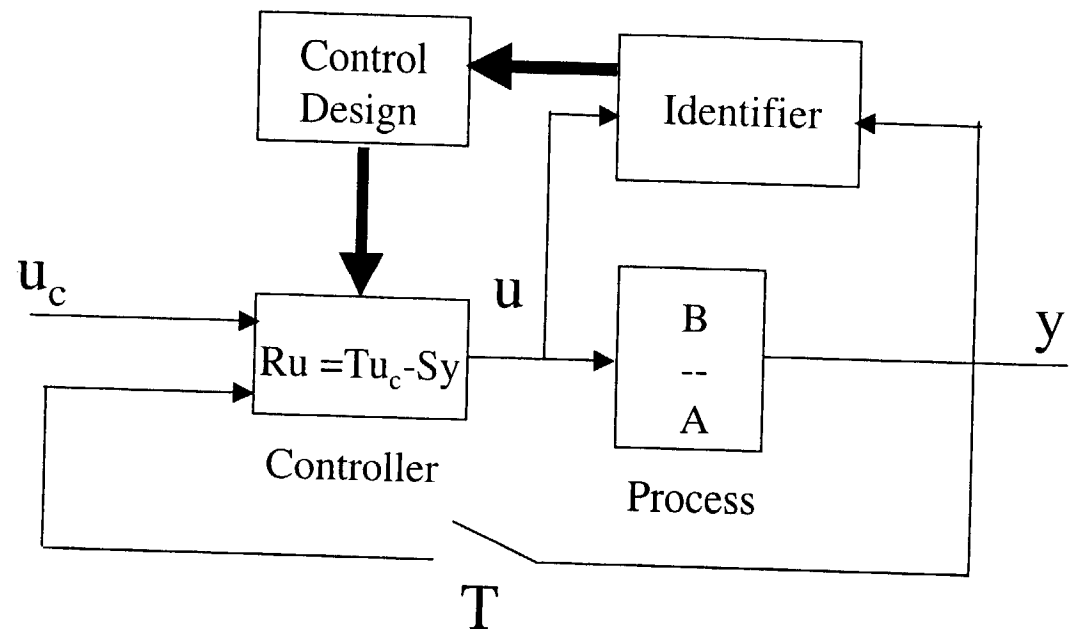
$$y(k) = \sum_{i=0}^n b_i u(k-i) - \sum_{i=1}^n a_i y(k-i)$$

The Identifier estimates the a_i and b_i coefficients which are used to calculate the r_i , t_i and s_i coefficients of the controller

When $n = 2$, the controller can be represented as a second order filter with an added set of terms for u_c

$$u(k) = t_0 u_c(k) + t_1 u_c(k-1) - s_0 y(k) - s_1 y(k-1) - s_2 y(k-2) - r_1 u(k-1) - r_2 u(k-2)$$

Where the relationship between the controller coefficients r_i , t_i and s_i and the estimated process parameters a_i and b_i is determined by the selection of a desired closed loop response and the pole placement design process





Self Tuning Controller



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- The identifier uses the recursive least-squares algorithm to estimate the process coefficients[1]

The model for the process can be expressed as $y(k) = \Phi^T(k-1)\Theta$

Where, for a second order system ($n = 2$),

$$\Theta^T = [a_1 \quad a_2 \quad b_0 \quad b_1]$$

$$\Phi^T = [-y(k-1) \quad -y(k-2) \quad u(k) \quad u(k-1)]$$

The least-squares estimator with exponential forgetting is

$$\hat{\Theta}(k) = \hat{\Theta}(k-1) + K(k)\varepsilon(k)$$

$$\varepsilon(k) = y(k) - \Phi^T(k-1)\hat{\Theta}(k-1)$$

$$K(k) = P(k-1)\Phi(k-1)(\lambda + \Phi^T(k-1)P(k-1)\Phi(k-1))^{-1}$$

$$P(k) = (I - K(k)\Phi^T(k-1))P(k-1)/\lambda$$



Self Tuning Controller



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- A PID controller can also be made adaptive by substituting it for the general linear controller used in the Self Tuning Controller development[16]
 - » The PID gains can be tuned on-line using a design approach that makes use of the estimated plant coefficients.
 - Dominant pole design is one such technique
 - Direct synthesis is another design approach (this is an Internal Model Control approach) [17]

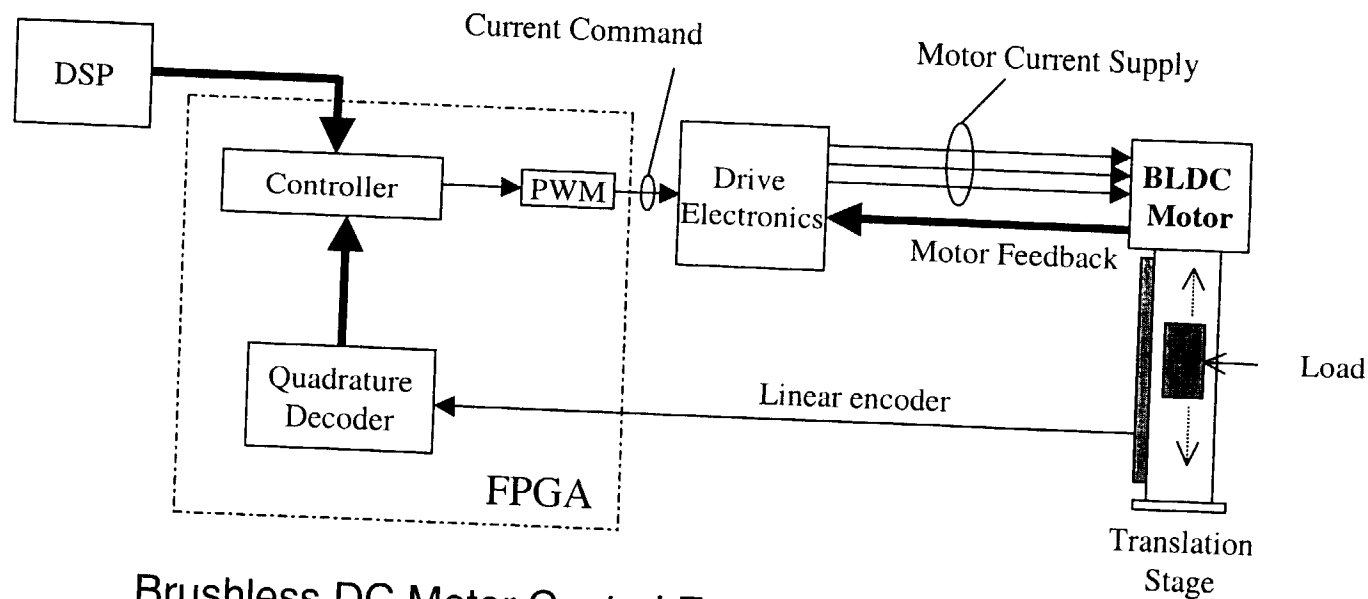


Experimental System



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- This work focuses on the application of adaptive control to Brushless DC motor-driven actuators
- The experimental system is diagrammed below
- This is a second order system; $n=2$ for the controller and identifier



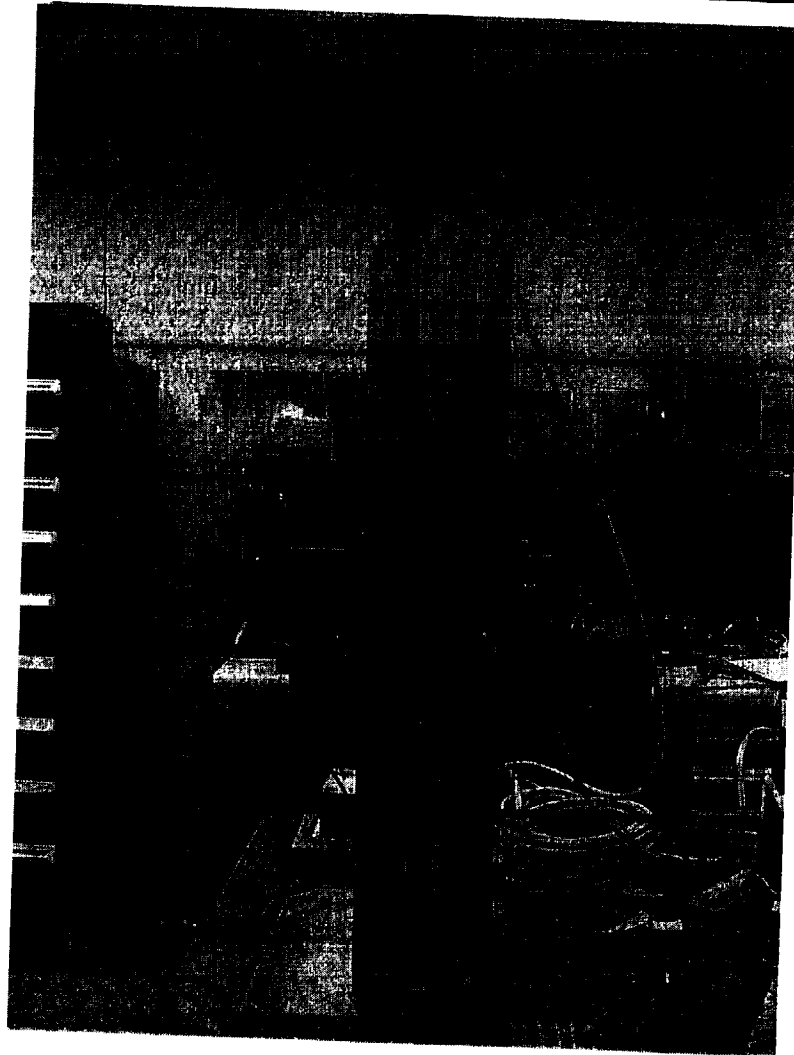
Brushless DC Motor Control Experimental Configuration



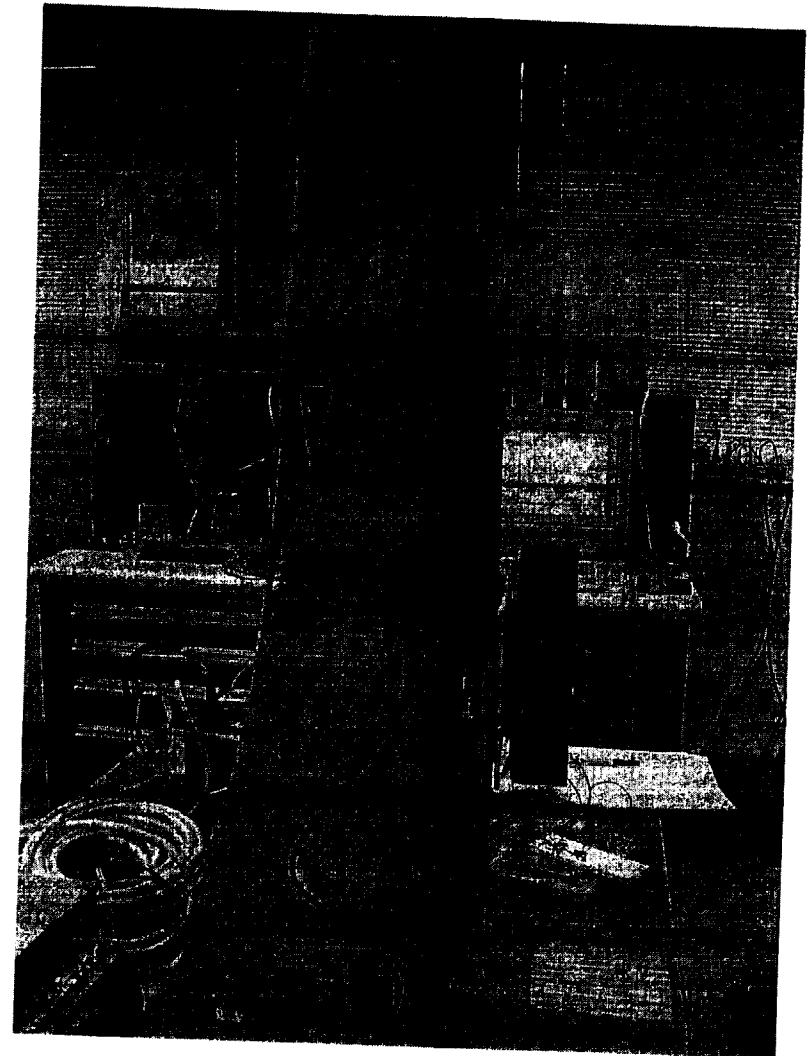
Experimental System



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P15



FPGA Implementation



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- Controller structures utilizing the digital filter representation can easily be implemented in an FPGA as this representation is simply a multiply-accumulate operation
- The estimator and the design functions require multiplication and division and are more complicated
- The controller requires peripheral functions to condition sensor measurement and control input to the plant
 - » Most of the required peripheral functions can be implemented as digital circuits on an FPGA.
 - » The peripheral functions will include a quadrature decoder/counter for position measurement and a PWM generator for motor current command
 - » An interface to a DSP will be used for desired trajectory commands and for configuration/capture of internal data

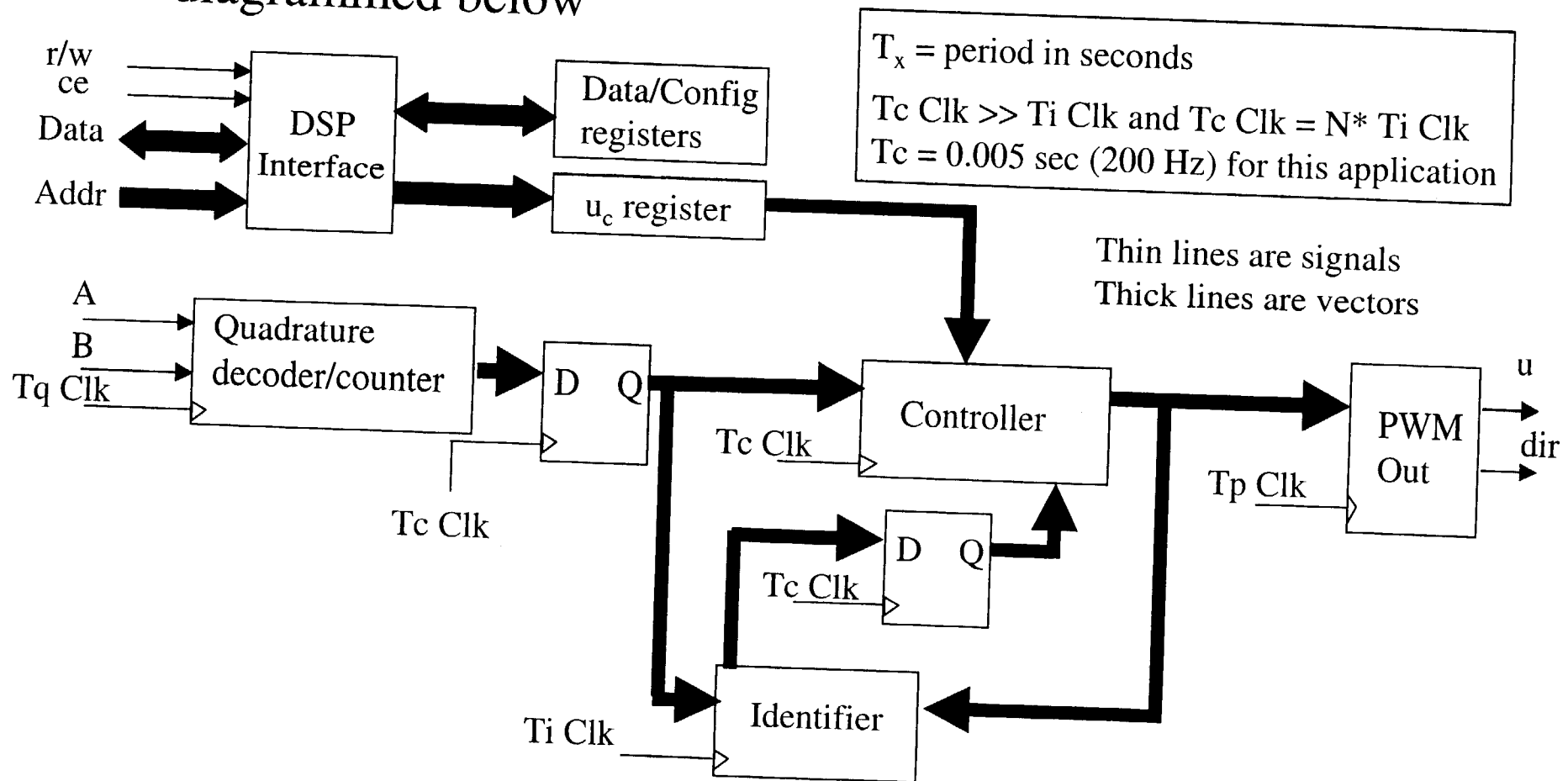


FPGA Implementation



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- The proposed FPGA implementation for this effort is diagrammed below



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Status



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- Currently the DSP Interface, Quadrature Decoder/Counter and PWM generator functions have been written in VHDL and implemented on a Xilinx Virtex XCV600 FPGA
 - » DSP Interface, Quadrature decoder, and 3 PWM generators consume 17% of the available logic resources and 17% of the available I/O blocks.
- These functions have been used by a controller implemented in software on the DSP to control the experimental system
- VHDL coding and testing of both a PID controller and a Pole-Placement controller is in progress
- Design and coding of the identifier and controller design blocks is in progress



Summary



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- Implementation of controllers as digital filters in FPGA's is feasible
 - » Literature contains many examples of controller implementations
 - » High order digital filters have been implemented on FPGA's[18,19,20]
 - » Capability for MHz clock rates provide plenty of processing capability, and controllers generally operate at sampling frequencies of much less than 10 kHz for most practical applications
- Implementation of the identifier and controller design calculations will be challenging, but should be feasible
 - » Identifier requires multiply and/or divide and accumulate
 - » Design equations have multiple variable terms and will require careful scaling
- Ultimately, the DSP interface will be replaced by a suitable communication interface for command and control



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